Multilayer Masking Technology for Fabricating Airborne CMUTs With Multi-Depth Fluidic Trenches

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***Abstract*— This paper presents a novel multilayer masking technology for fabricating airborne capacitive micromachined ultrasonic transducers (CMUTs) with multi-depth fluidic trenches, in which a plurality of masking layers for different etch depths are selectively patterned prior to the real etching to keep a planar wafer surface. The multi-depth fluidic trenches are utilized to effectively control the squeeze film within the CMUT gap and tune the fractional bandwidth (FBW) of CMUT. As such, the FBW can be changed over a wide range by only adjusting the trench height. With further lowering the gap height, the FBW can be extremely widened up to 168%. The receive sensitivity has also been significantly improved through the process of local oxidation of silicon to reduce the parasitic capacitance. The proposed multilayer masking technology enables the fabrication of airborne CMUTs with different FBWs and sensitivities on the same wafer and further combine these devices into arrays for high-resolution imaging and photoacoustic or thermoacoustic applications. These devices also provide a low minimum detectable pressure (MDP), as low as 1.37 mPa in the FBW of 13.5% for the 8.5 μm deep fluidic trenches and 1.52 mPa in the 17.2% FBW for the 16.2 μm trenches. Furthermore, the multilayer masking technology demonstrates the capability of building microelectromechanical systems (MEMS) with multi-depth micro/nanostructures. [2021-0090]**

***Index Terms*— Microelectromechanical systems (MEMS), capacitive micromachined ultrasonic transducers (CMUTs), multilayer masking technology, squeeze film, multi-depth fluidic trenches, ultra-wide bandwidth.**

I. Introduction

CAPACITIVE Micromachined Ultrasonic Transducers (CMUTs) have emerged as an alternative to piezoelectric transducers, offering advantages such as wide bandwidth, ease of fabricating large arrays, and easy integration with supporting electronic circuits. As such, CMUTs are ideal for applications in medical imaging, therapeutics, chemical sensing, and air-coupled ultrasound. In airborne applications such as non-contact thermoacoustic root imaging, both wide bandwidth (BW) and high sensitivity are desired for improving resolution and overcoming the 65 dB interface loss due to the impedance mismatch at the air-sample boundary. More than 3.5% of the bandwidth is required for the non-contact thermoacoustic imaging system, while the sensitivity should be as high as possible to increase the detection distance [1], [2]. Conventional vacuum CMUTs have high sensitivity but with limited BW [3]. To widen the BW, a gaseous squeeze film was introduced by perforating [4]–[6]. However, perforating either the plate or the substrate to vent the cavity and manipulate the squeeze film results in a significant decrease in sensitivity and dramatic increase in the pull-in voltage, and generates strong harmonics by transducers' mounting and housing [5], also brings significant acoustic loss through the perforating holes [4]. We have demonstrated a novel method in the literature [7], in which squeeze film is introduced and tunned within a submicron gap by creating optimal fluidic trenches and through-wafer vias in the substrate. Therefore, the BW of CMUT can be significantly broadened and effectively controlled by merely changing the trench height while obtaining high sensitivity and keeping low driving voltage. Almost no energy leaks from the narrow through via, which guarantees a super low acoustic loss.

However, conventional lithography and etching techniques are not suitable for fabricating those devices with multi-depth fluidic trenches and through-wafer vias. Lithography in deep trenches would become very challenging, and the patterning accuracy cannot be guaranteed. In the meanwhile, photoresist would be trapped in the through-wafer vias and cannot be removed completely, which makes the subsequent processes such as thermal oxidation undoable. The emerging multilayer hard mask technology for 3D micro/nanofabrication provides a feasible solution. Frommhold *et al.* utilized multilayer hard mask stacks for high resolution and high-aspect-ratio etching [8]. Abe *et al.* explored a dry etching method using double-layered mask for modulating surface shape of 3D microstructures [9]. Han *et al.* demonstrated metal oxide multilayer masks for 3D nanofabrication [10]. Li *et al.* presented a nanofabrication technique on unconventional substrates using transferred hard masks [11].

In this paper, we present a novel multilayer masking technology wherein a plurality of hard mask layers for different etch depths are selectively patterned prior to the real etching to keep the wafer a planar surface. Therefore, the patterning accuracy and the achievability of the whole fabrication can be guaranteed. Combining local oxidation of silicon (LOCOS)

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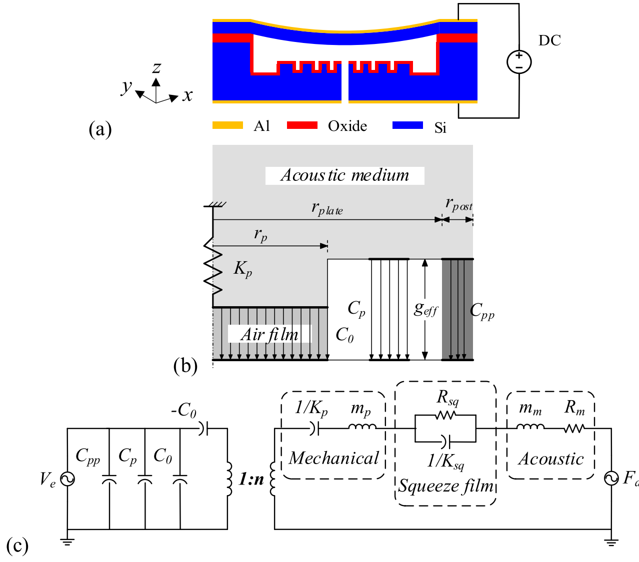

Fig. 1. (a) Schematic of the vented CMUT with fluidic trenches and a through via, and (b) the equivalent lumped piston model and (c) the equivalent circuit.

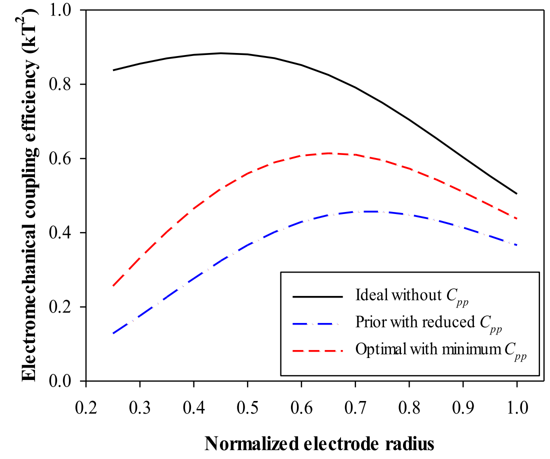

Fig. 2. Electromechanical coupling efficiency versus the normalized electrode radius and parasitic capacitance.

process and wafer bonding technique, the fabrication flow has been optimized to significantly improve the sensitivity of the built transducers. Finally, the vented CMUTs with multi-depth fluidic trenches and through-wafer vias have been built and tested. A conventional vacuum CMUT has also been fabricated with sharing process steps to obtain extremely high sensitivity and wide range frequency adjustment.

II. Optimization of Airborne CMUTs

A conventional CMUT is an electrostatically actuated variable capacitor that couples to an acoustic medium. The electrostatic force is modulated by an alternating current (AC) and harmonically pulls and pushes the moveable plate of the capacitor, hence generating an ultrasound wave into the surrounding medium. When an ultrasound impinges on the moveable plate, the caused vibration changes the active capacitance hence generates an electric current, then is converted into a voltage through the receiving electronics.

A. Equivalent Modeling

A CMUT can be modeled as an equivalent lumped piston [12], [13], and further simplified as a small-signal equivalent circuit [14], [15]. As Fig. 1 (b) shown, the moveable plate is presented with an equivalent spring K_p and a mass m_p. The total capacitance is divided into an active capacitance C_0 and a parasitic capacitance C_p. There's another dominating parasitic capacitance C_{pp} from the post area that is used to anchor the moveable plate. To improve the receive sensitivity, it's better to make a CMUT behaving as a piston transducer. Ideally, the electromechanical coupling efficiency increases with shrinking the area of electrode and gets the maximum value of 0.88 at the normalized radius of 0.45 and biased with 90% of the pull-in voltage, as shown in Fig. 2. However, an insulation layer is required to cover both the cavity region and the post area in a real fabrication. To significantly reduce the dominating parasitic capacitance C_{pp}, a 1.0 μm thick silicon oxide layer is formed in our prior design [7]. With adding this uniform insulation layer, the maximum coupling efficiency significantly drops to less than 0.46 while the normalized radius shifts to 0.7. Benefiting by the proposed multilayer masking technology and the local oxidation of silicon process, we can form a thinner silicon oxide layer with only 0.2 μm thick over the cavity region but maximize it to be 2.0 μm at the post area to improve the coupling efficiency and minimize the parasitic capacitance C_{pp}. Combining with etching away the nonactive cavity region, the electromechanical coupling efficiency has been improved to 0.61 in the recent optimal design, which is around 33% over our prior design.

As presented in the literature [7], we introduce a gaseous squeeze film damping mechanism to broaden the bandwidth of CMUT. Fig. 1 (a) shows that the CMUT cavity is vented through by a small via at the center. The air squeeze film is introduced into the cavity between the moveable plate and the solid substrate, and effectively controlled by the optimal fluidic trenches in the substrate. To simplify the analysis of the squeeze film damping effect, it is modeled as a lumped spring-damping mechanical system and eventually converted into a resistor R_{sq} in parallel with a capacitor K_{sq} in the equivalent circuit. Therefore, the fractional bandwidth can be derived from the equivalent circuit and written as [5], [14]

$$FBW = \frac{R_m + R_{sq}}{\sqrt{m_{tot} K_{tot}}}, \tag{1}$$

where the damping load R_m and R_{sq} are from air medium and the squeeze film, respectively. The total mass m_{tot} includes the medium mass and the equivalent piston mass, while the total spring stiffness K_{tot} consists of the stiffness of the equivalent piston, the electrostatic spring softening effect, and the stiffening effect of the squeeze film. For frequencies lower than the cutoff frequency, the squeeze film acts as a viscous damper with the damping constant $b_{sq} R_{sq}$, while for frequencies higher than the cutoff frequency, the squeeze film acts as a spring K_{sq}. Therefore, the FBW can be controlled by tuning

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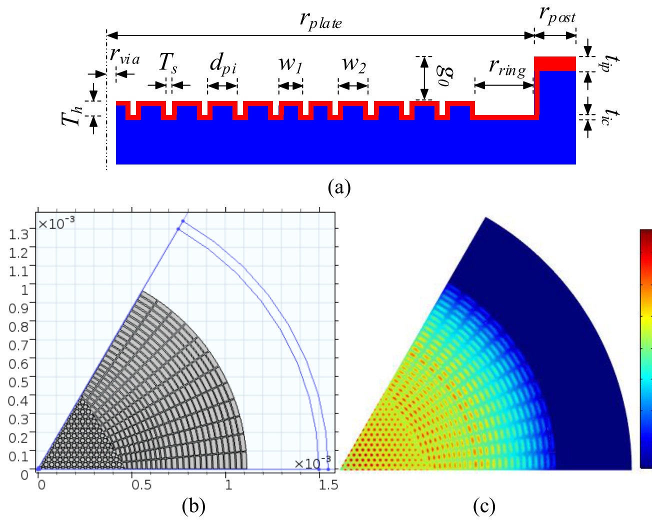

Fig. 3. Hybrid fluidic trenches with micropillar array at the center and fan-shaped trenches at the periphery. (a) Schematic (not in scale) and (b) the trench distribution, and (c) the absolute pressure (in Pascal) on the surface of the substrate electrodes.

TABLE I
DESIGN PARAMETERS OF THE VENTED CMUTs

Parameter		Value (μm)
Plate radius: r_{plate}		1500
Plate thickness: t_{plate}		50.0
Radius of the post area: r_{post}		50.0
Gap height: g_0		0.9
Thickness of insulation oxide	in the cavity: t_{ic}	0.25
	at the post area: t_{ip}	2.0
Radius of etch ring: r_{ring}		384
Radius of through-wafer via: r_{via}		10.0
Diameter of micropillar: d_{pi}		24.0
Width of fan-shaped electrode:	w_1	20.0
	w_2	25.0
Trench spacing: T_s		6.0
Trench height: T_h		2.0 ~ 15.0

the squeeze film damping and stiffening effects. The so-called spring softening effect, which originates from the nonlinear electrostatic force, has a significant impact on the CMUT sensitivity and FBW. It's converted to $-C_0$ in the equivalent circuit by moving it to the electrical side, and given by

$$K_{soft} = \frac{n^2}{C_0}, \tag{2}$$

where $n = E_0 C_0$ represents the electromechanical transformer ratio, E_0 is the electrical field within the gap of CMUT.

B. Optimization of Fluidic Trenches

The cavity of CMUT is vented by a through-wafer via at the center with a radius of less than 10 μm. This optimal design guarantees low acoustic loss and does not sacrifice the sensitivity [17]. The gap is reduced to submicron by optimizing the hybrid fluidic trenches in the substrate, which effectively tune the squeeze film and control the bandwidth. Fig. 3 (a) shows the optimal hybrid fluidic trenches, which consists of micropillar array at the center and fan-shaped trenches at the periphery of the CMUT cell. The stiffening effect dominates the behavior of the squeeze film when the gap is lower than one micron and causes the resonant frequency increasing significantly. The micropillar array with a similar octagonal distribution of perforated holes can significantly lower the stiffening effect and keep the resonant frequency as designed [18]–[21]. As Fig. 3 (b) shown, the absolute pressure on the surface of the substrate electrodes, which is obtained by COMSOL Multiphysics® simulation software, is consequently lowered to one-tenth of that of flat substrate without fluidic trenches. To improve the pressure uniformity and further increase the electrode ratio, fan-shaped trenches are introduced at the periphery, in which the electrode area can be adjusted linearly with the radius [7]. The specific design parameters for the micropillars and the fan-shaped trenches were optimized by the multi-parameter optimization method [17]. The objective is to get a low and uniform absolute pressure on the substate and lower the resonance frequency to the desired value. This can be achieved by looking for an optimal parameter combination of the control variables such as the radius of the micropillar, the trench spacing, and the width of the fan-shaped electrodes. The specific parameters are shown in Table I. Finally, the hybrid fluidic trenches reduce the stiffening effect most effectively while maintaining a large electrode ratio as much as of 86% and a minimum pull-in voltage.

After optimizing the geometry and distribution of the fluidic trenches, the trench height is used as a unique variable to tune the damping effect, and thus, control the bandwidth of CMUT. However, the pull-in voltage does not change with the trench height due to the fixed area of the substrate electrodes. The pull-in voltage has been lowered to less than 33.5 V with a 0.9 μm gap, which makes airborne CMUTs applicable for smart wearable or implantable devices that require low power consumption. By increasing trench height from 2.0 μm to 15.0 μm, the bandwidth has been significantly improved more than 2.3 times from 3.6% to 11.9% with a DC bias of 90% of the pull-in voltage, while the sensitivity only got worse than 32% from 7.6 mV/Pa to 5.2 mV/Pa, as shown in Fig. 4 (a). The FBW can be further widened up to 18.0% by increasing the DC bias to be of 99% of the pull-in voltage. Generally, sensitivity and bandwidth are a trade-off parameter pair, *i.e.,* increasing bandwidth will degrade sensitivity. However, in our optimal designs, by adjusting the trench height to control the bandwidth, the sensitivity-bandwidth product is increased significantly more than 1.2 times.

To reduce the parasitic capacitance from the CMUT itself, the nonactive region with the width of around one third of the radius is etched much deeper. The insulation layer of silicon oxide at the post region has been maximized within the limitation of fabrication capacity to significantly reduce the parasitic capacitance and improve the electromechanical coupling efficiency. As Fig. 4(a) shown, the voltage receive sensitivity has got improved more than 40% over our previous design, and the pull-in voltage has been further lowered more than 38%.

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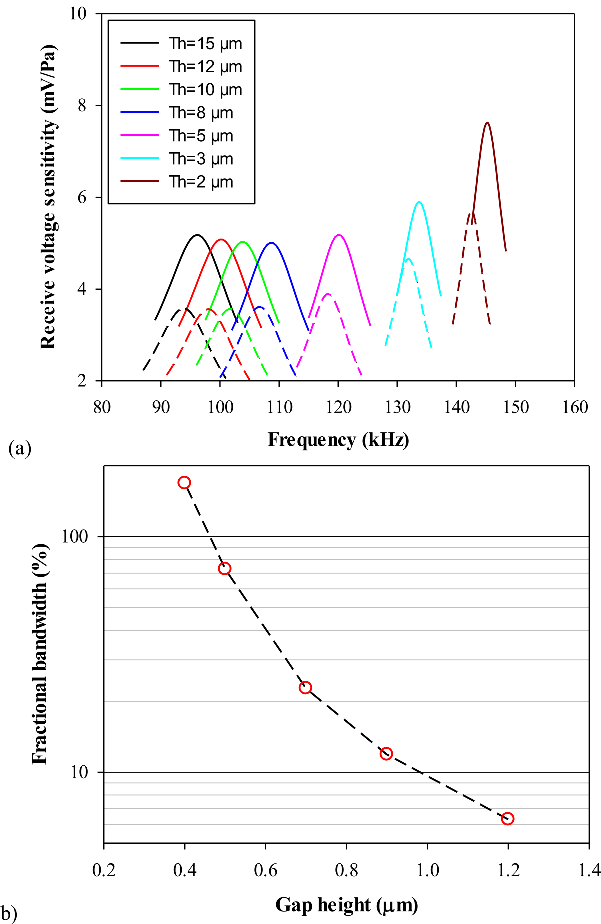

Fig. 4. (a) Receive voltage sensitivity versus frequency (dashed lines are for our previous designs [7]), and (b) fractional bandwidth versus gap height.

With decreasing the gap height further, the bandwidth can be widened extremely and achieve ultra-wide bandwidth. When the gap is lowered to 0.4 μm, the bandwidth is widened to more than 168%, as shown in Fig. 4 (b), while the pull-in voltage drops to less than 11 V. However, the resonance frequency doesn't change much, and still maintains high sensitivity.

III. Fabrication

To verify the design theory, we are going to fabricate the designs with 8 μm and 16 μm deep fluidic trenches on a single wafer. However, in a conventional fabrication flow, the 8 μm trenches would be formed at first and then the 16 μm trenches. Therefore, a lithography using thick photoresist must be done in the etched 8 μm trenches, which brings challenges for photoresist coating and exposure, and the patterning accuracy cannot be guaranteed. It becomes even harder to successfully complete the patterning in the 16 μm trenches. Thereafter, it's impossible to do patterning in the small through-wafer vias, which is typically smaller than 20 μm and deeper than 200 μm. Otherwise, the photoresist would be trapped in the vias and cannot be removed completely, which makes the subsequent processes such as thermal oxidation undoable.

We have developed a novel microfabrication process that is based on multilayer masking technology, local oxidation, and direct wafer bonding, in which all various CMUT designs

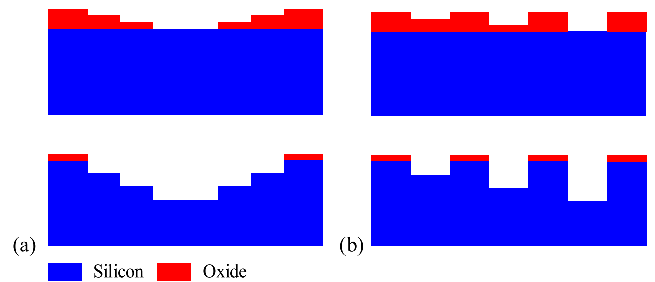

Fig. 5. Multilayer masking technology for etching of (a) a single multi-step structure and (b) multiple structures with multi-depths.

with different trench heights, all within the desired bandwidth can be built on a single wafer and further combine these devices into arrays for high-resolution imaging and photoacoustic or thermoacoustic applications. Meanwhile, the proposed process has significantly reduced the parasitic capacitance and improved the receive sensitivity.

A. Multilayer Masking Technology

A novel multilayer masking technology for etching multi-depth microstructures is presented, in which a plurality of hard mask layers for different etch depths are patterned prior to the etching of silicon wafer. As Fig. 5 shown, the proposed processes eliminate any photolithography steps once the real etching has begun and keep the wafer a planar surface. Here, silicon oxide is selected as the masking material, which can be easily formed by Low Pressure Chemical Vapor Deposition (LPCVD) or thermal oxidation and etched by Reactive Ion Etching (RIE). The masking layer is divided into a plurality of layers and selectively patterned by photolithography and RIE etching to form masks for areas where different silicon etch depths are desired. Then, the wafer is etched by deep RIE to a first level, following by removing the remaining mask of this layer through precise dry etching. Again, the wafer is etched to another level with the remaining masks. The process is repeated until all the desired levels have been etched in the silicon wafer. Fig. 5 shows the two different microstructures that can be achieved by the proposed multilayer masking technology: one is for the single multi-step structure; the other is for the multiple structures with different depths.

To tune the BW of airborne CMUT, fluidic trenches with different depths are introduced to manipulate the squeeze film within the submicron gap. Therefore, Fig. 5(b) demonstrates a feasible fabrication method to build our airborne CMUTs with the optimal multi-depth fluidic trenches.

B. Local Oxidation and Direct Wafer Bonding

Traditionally, the insulation layer across the cavity and the post area is uniform. Therefore, it must be thickened uniformly to reduce the parasitic capacitance, which results in a significant increase of the pull-in voltage. To significantly reduce the parasitic capacitance and improve the receive sensitivity, local oxidation of silicon (LOCOS) is introduced, which obtains a thinner insulation layer in the cavity but much thicker at the post area. This maintains a low pull-in voltage, however, achieves very small parasitic capacitance. The LOCOS process

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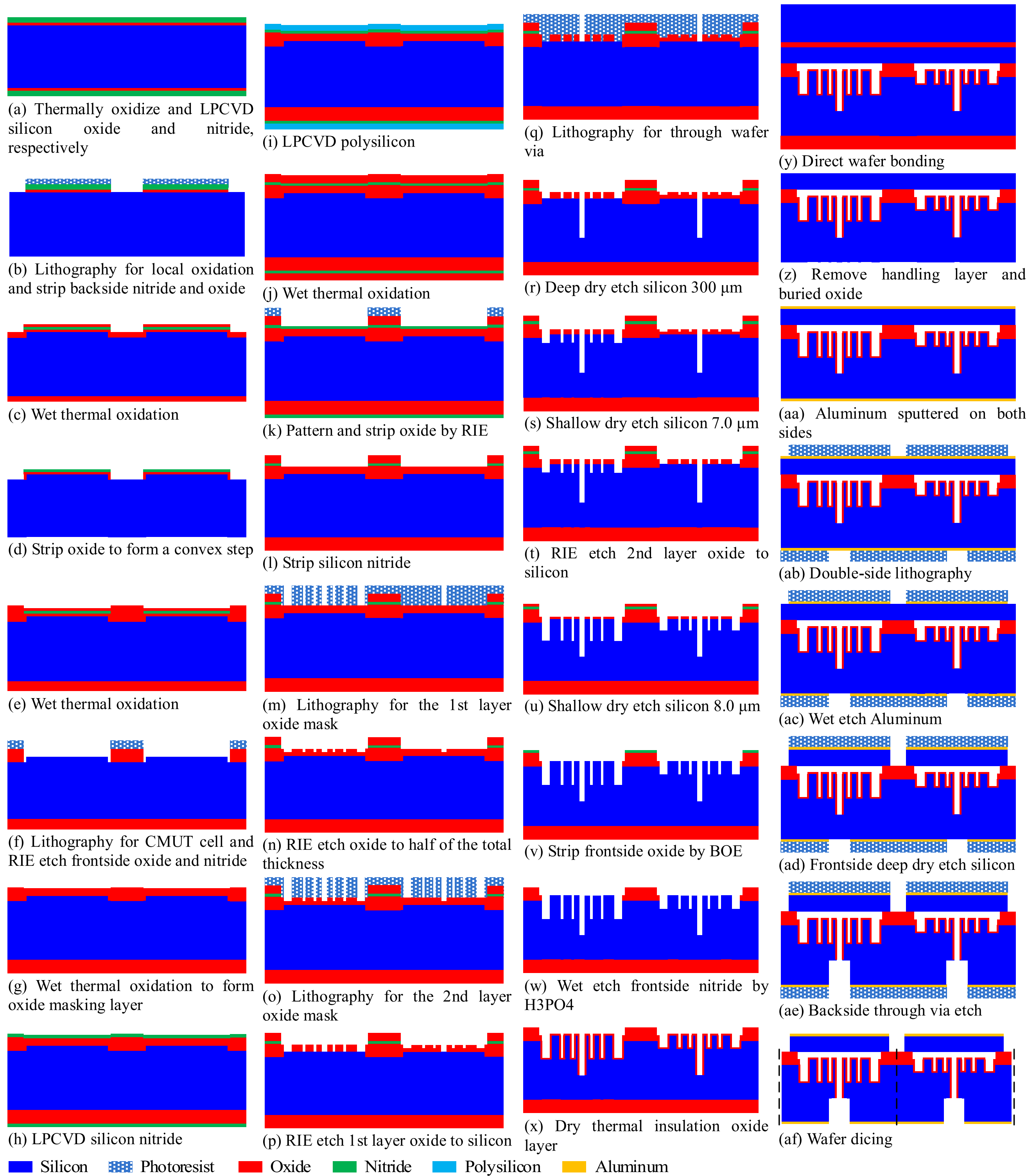

Fig. 6. Fabrication flow with the proposed multilayer masking technology, local oxidation of silicon and direct wafer bonding techniques.

provides a precise control of the oxidation thickness that can be used to form a thin gap [22], [23]. It also provides excellent roughness control and unprecedented uniformity across the whole wafer, which is required for direct wafer bonding. The direct wafer bonding provides the advantages of simple fabrication, good uniformity, and low intrinsic stress. Herein, we adopt the LOCOS wafer-bonding process combining with the multilayer masking technology to build our airborne CMUTs. Compared with our previous fabrication, the parasitic capacitance is reduced by 60%, which signicantly improves the receive sensitivity more than 40%. The pull-in voltage is also lowered by around 40%.

C. Fabrication Flow

The fabrication flow is shown in Fig. 6. The specific processing details are described by the following key steps:

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1) Formation of Cavity: First, as Fig. 6 (a) shown, one passivation layer of silicon oxide is formed by thermal oxidation and followed by one barrier layer of silicon nitride deposited by LPCVD. Then, these two layers are patterned, and the protected regions define the cavities of the airborne CMUTs (Fig. 6 (b)). Laterally, thermal oxidation is proceeded to form a convex step with 0.8 μm deep after removing the oxide layer (Fig. 6 (d)). The step height can be accurately controlled by this oxidation process. Another time oxidation is done to form a 2.0 μm thick oxide at the bonding area (Fig. 6 (e)). The thick oxide significantly reduces the parasitic capacitance and improves the receive sensitivity. Then, the masking nitride and oxide layers are removed, as Fig. 6 (f) shown. Another oxidation layer is formed at the cavity regions to use as the multiple masking layers for trenches etching (Fig. 6 (g)). The final gap height is determined and precisely controlled by the previous oxidation processes. Then, one layer of silicon nitride is deposited by LPCVD to protect the bonding surface for future direct wafer bonding (Fig. 6 (h)).

A vacuum device with excellent receive sensitivity but narrow bandwidth is built as well for improving the non-contact detection distance. The fabrication shares most of the above processes including the formation of cavity, direct wafer bonding, and plate etching. However, the cavity gap was etched further deeper to be 6.2 μm by RIE. The deflection of CMUT plate caused by the atmospheric pressure is around 5.5 μm. The actual gap height for the vacuum device is only 0.7 μm, which guarantee the super-high sensitivity and low pull-in voltage.

2) Patterning of Fluidic Trenches: Next, one layer of polysilicon is deposited and oxidized to use as the masking layer to protect the bonding region (Fig. 6 (i-j)). This oxide layer and the protecting nitride layer at the cavity regions is then removed by Buffered Oxide Etch (BOE) and Phosphoric acid (H3PO4), respectively, as shown in Fig. 6 (k-l). The oxide masking layer is virtually divided into two equal layers with half of the total thickness. The first layer is patterned for etching the 15 μm deep trenches (Fig. 6(m)) and transferred into the oxide layer by dry etching half of the total thickness, as shown in Fig. 6 (n). The second layer is patterned and etched thereafter for the 8 μm deep trenches in the same way with the first masking layer (Fig. 6 (o-p)).

3) Frontside via and Fluidic Trenches Etching: To etch a through-wafer via with a small radius, the etching process is divided into the frontside etching and the backside etching. The frontside via is patterned and then etched 300 μm by deep RIE etching from the frontside (Fig. 6 (q-r)). The radius of the through via is set to 10 μm, which guarantees super low acoustic loss but without sacrificing the bandwidth and sensitivity of the airborne CMUT.

After finishing front via etching, the silicon is etched 7.0 μm deep with the first masking oxide layer, as shown in Fig. 6 (s). Then, the remaining thickness of the second masking oxide layer, which covers the fluidic trenches regions, is etched off (Fig. 6 (t)). The silicon is then etched another 8.0 μm deep (Fig. 6 (u)). The 15 μm and 8 μm deep fluidic trenches are accurately etched by RIE to manipulate the squeeze film and control the bandwidth. The proposed oxide multiple masking layers guarantee the accuracy of the geometry patterning and fluidic trenches etching. Also, no patterning occurs in the deep trenches and through-wafer vias, thus no photoresist would be trapped in the through vias. Otherwise, the trapped photoresist would destroy the oxidation furnace in the subsequent steps. Fig. 7 shows the SEM micrograph of the through vias and the hybrid fluidic trenches consisting of the micropillar array trenches at the center and the fan-shaped hybrid trenches at the periphery of the CMUT cell. The maximum variation for the trench etching was controlled to less than 3%.

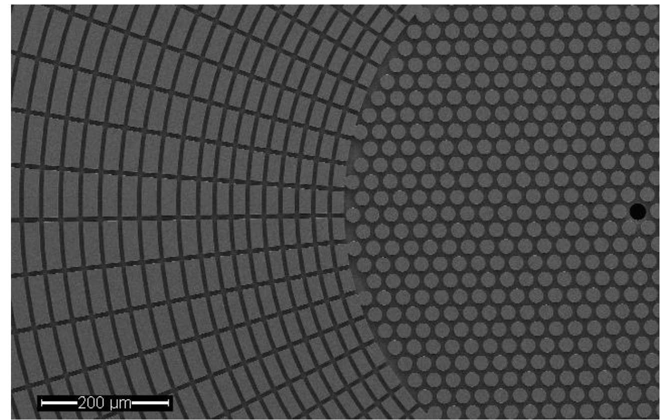

Fig. 7. SEM micrograph of the hybrid fluidic trenches (partial): vented through via, micropillar array at the center and fan-shaped trenches at the periphery.

4) Direct Wafer Bonding: The frontside oxide layer is etched away by BOE (Fig. 6 (v)), and the frontside nitride is stripped by H3PO4 (Fig. 6 (w)) to keep the roughness of the bonding area to be as low as possible. As Fig. 6 (x) shows, 300 nm thick oxide layer is dry thermally grown as an insulating layer to prevent short circuiting. The processed wafer is then bonded to a silicon-on-insulation (SOI) wafer (Fig. 6 (y)) using the direct fusion bonding techniques [24], which provides the advantage of low residual stress and good uniformity of the plate thickness. Fig. 8 shows the roughness of the bonding surfaces measured by Atomic Force Microscope (AFM). The original surface roughness of the device layer of the SOI wafer is only 0.9 Å. The surface roughness of the substrate oxide at the bonding region is 2.7 Å, which guarantees a successful direct wafer bonding.

After fusion bonding, the handling and buried oxide layers of the SOI wafer are removed by 30% KOH solution and buffered HF, respectively, as shown in Fig. 6 (z).

5) Plate Etching and Cavity Venting: A 300 nm thick layer of aluminum is sputtered on both front and back sides of the bonded wafer to provide better electrical contacts (Fig. 6 (aa)). Then double-side lithography is proceeded to pattern both CMUT cells and through-wafer vias, as Fig. 6 (ab-ac) shows. The excess silicon surrounding the CMUT cells is etched away to reduce the parasitic capacitance (Fig. 6 (ad)). To vent the cavity of CMUT, the backside through-wafer vias are etched through deep RIE (Fig. 6 (ae)). Finally, the wafer is diced into single CMUT elements, as shown in Fig. 6 (af). The Table II lists the critical parameters of the vacuum and vented CMUTs built from the real fabrication.

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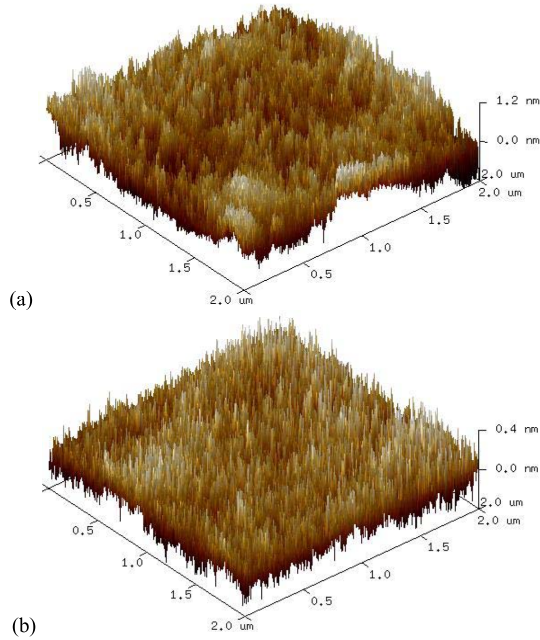

Fig. 8. AFM roughness of the bonding surfaces: (a) substrate oxide surface with 2.7 Å roughness and (b) silicon plate surface of SOI wafer with 0.9 Å.

TABLE II
PARAMETERS OF THE BUILT VACUUM AND VENTED CMUTs

Parameter	Value		
	Vacuum CMUT	Vented CMUTs	
Plate radius (μm)	1500		
Plate thickness (μm)	50.9	50.2	
Insulation oxide thickness (nm)	253	299	
Bonding oxide thickness (μm)	2.00	2.27	
Gap height (μm)	6.23	0.85	
Trench height (μm)	0	8.5	16.2

The vacuum device shares the same wafer bonding and plate etching processes but didn't be etched from the backside which would vent the cavity.

IV. CHARACTERIZATIONS

Electrical impedance and maximum displacement sensitivity measurements have been conducted to verify the design theory. The electrostatic softening effect has been investigated to improve the sensitivity and widen the bandwidth.

A. Electrical Impedance and Minimum Detectable Pressure

Fig. 9 shows the measured amplitude and phase of the electrical impedance for the vacuum and vented CMUTs, respectively. The measured pull-in voltage for the vacuum CMUT is around 67 V, which agrees well with the simulation value of 69.5 V. However, the measured pull-in voltages for the vented CMUTs are approximately 12.5% of higher than the simulations, which is due to the larger gap caused by the residual stress in the SOI wafer. The residual stress makes the fabricated plate bowed up around 100 nm after venting the CMUT cavity.

The electrical impedance measurements show that both the vacuum and vented CMUTs have a strong electrostatic softening effect with increasing the DC bias. For the vacuum CMUT,

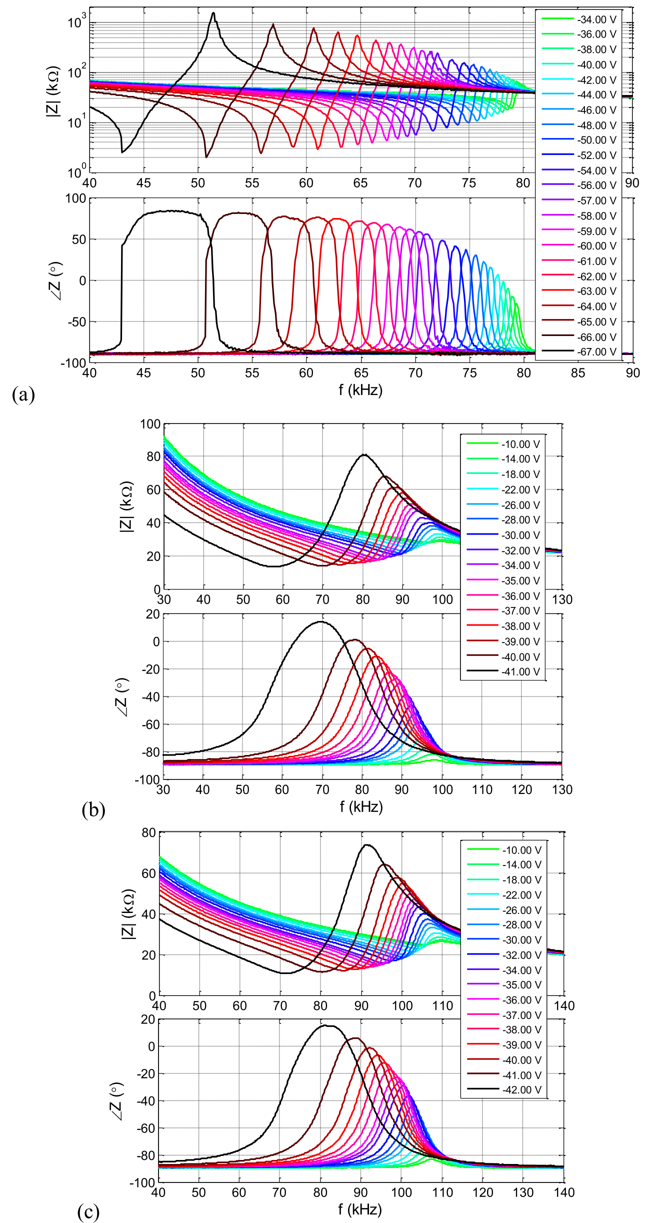

Fig. 9. Measured impedance of (a) the vacuum CMUT and the vented CMUT (b) with 16.2 μm deep trenches and (c) with 8.5 μm deep trenches.

the resonance frequency can be tuned in a wide range from 80 kHz to 40 kHz with only changing the DC bias, and the sensitivity has been significantly improved by increasing the DC bias. With combing the same individual vacuum CMUTs into an array and controlling the DC bias to tune the resonance frequency, we can obtain ultra-wide bandwidth and super-high sensitivity at the same time. In the literature [25], [26], Kupnik *et al.* designed a CMUT array with different sizes connecting in parallel to get a larger bandwidth at the expense of gain and transducer size. For the vented CMUTs, the resonance frequency also can be changed in a large range of 40 kHz by adjusting the DC bias. However, the squeeze film dominates the performance of the vented CMUT and gives much wider bandwidth than the vacuum CMUT. Through only adjusting the trench height, the resonance frequency and the bandwidth have been tuned, as Fig. 9 (b) and (c)

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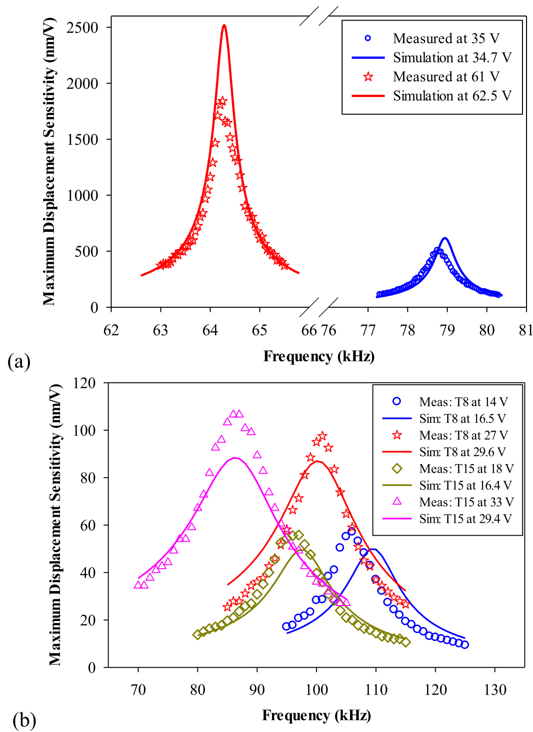

Fig. 10. Measured maximum displacement sensitivity of (a) the vacuum CMUT and (b) the vented CMUTs with 16.2 μm and 8.5 μm deep trenches.

shown. The resonant frequency decreases with increasing the trench height, resulting from the reduced stiffening effect of the squeeze film. Compared with the vacuum CMUT, the individual vented CMUT has much wider bandwidth, and the bandwidth can be controlled by the height of the fluidic trenches, which benefits from the introduced squeeze film damping mechanism. Furthermore, the driving DC can finely tune the bandwidth further by controlling the thickness of the squeeze film. With adjusting the DC bias, an individual vented CMUT can provide ultra-wide bandwidth, also high sensitivity compared with conventional vented CMUTs.

The minimum detectable pressure (MDP) in receive mode, is associated with the noise contribution of the medium damping and the squeeze film damping. It is determined by $P_{in,\min} = \sqrt{4k_B T(R_m + R_{sq})}/A_{plate}$. k_B is the Boltzmann constant, T is the temperature, and A_{plate} represents the equivalent area of the plate. The additional squeeze film damping has siginificantly widened the bandwidth, but also increased the MDP. Based on the measured impedance and the calculated electromechanical transformer ratio based on the simulation results, the MDP driving at 95% of pull-in voltage for the built vacuum CMUT is 0.94 μPa/$\sqrt{}$Hz, and 6.43 μPa/$\sqrt{}$Hz with a 14.4 kHz bandwidth for the vented CMUT with 8.5 μm fluidic trenches and 6.74 μPa/$\sqrt{}$Hz with a 16.1 kHz BW for the 16.2 μm trenches.

B. Maximum Displacement Sensitivity

As Fig. 10 shows, the measured displacement sensitivity for both the vacuum and vented CMUTs matches the simulation results very well. The main errors come from the misaligned center point of the CMUT plate and the electrical noise. The sensitivity of the vacuum CMUT gets improved significantly from 506 nm/V to 1840 nm/V by increasing the DC bias from 50% to 90% of pull-in voltage. The measured bandwidth is a little bit wider than the theory due to the induced small packaging damping when bonding CMUT on a PCB substrate. For the vented CMUTs, the maximum displacement sensitivity biased at 90% of the pull-in voltage is more than 100 nm/V, which is significantly suppressed by the squeeze film damping compared with that of the vacuum CMUT. The bandwidth has been widened from 7.9% to 12.8% when increasing the trench height from 8.5 μm to 16.2 μm. However, the measured bandwidth is a little bit narrower than the theoretical values. Here, the packaging damping is negligible compared to the squeeze film damping. The main error is from the enlarged gap caused by the bowed-up plate due to the residual stress in the SOI wafer. Overall, the fractional bandwidth can be easily controlled from less than 1% to more than 17% by introducing the squeeze film damping mechanism and adjusting the trench height, also can be finely tuned by the DC bias further.

V. Conclusion

We have proposed a novel multilayer masking technology to fabricate airborne CMUTs with ultra-wide bandwidth and high sensitivity. The multilayer masking technology guaranteed the fabrication of the multi-depth fluidic trenches, in which the trench height was uniquely used to control the bandwidth through tuning the stiffening and damping effect of the squeeze film between the gap of CMUT. The simulation results show that the bandwidth can be further widened up to 168% by thinning the squeeze film to less than 0.4 μm, while lowered the driving voltage to less than 10 V. Combined with local oxidation and direct wafer bonding techniques, the various CMUTs with different trench heights have been successfully fabricated on one single wafer, which shows the capability of further combining these devices into arrays for high-resolution imaging and photoacoustic or thermoacoustic applications. The local oxidation has significantly reduced the parasitic capacitance and improved the receive sensitivity. The measured electrical impedance and maximum displacement sensitivity agree well with the finite element simulations, which certify the design theory and the fabrication method. Furthermore, the proposed multilayer masking technology demonstrates the capability of building MEMS devices with multi-depth micro/nanostructures.

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References

[1] H. Nan *et al.*, "Non-contact thermoacoustic detection of embedded targets using airborne-capacitive micromachined ultrasonic transducers," *Appl. Phys. Lett.*, vol. 106, no. 8, Feb. 2015, Art. no. 084101.

[2] A. Singhvi, K. C. Boyle, M. Fallahpour, B. T. Khuri-Yakub, and A. Arbabian, "A microwave-induced thermoacoustic imaging system with non-contact ultrasound detection," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 66, no. 10, pp. 1587–1599, Oct. 2019.

[3] K. K. Park and B. T. Khuri-Yakub, "3-D airborne ultrasound synthetic aperture imaging based on capacitive micromachined ultrasonic transducers," *Ultrasonics*, vol. 53, no. 7, pp. 1355–1362, 2013.

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[4] N. Apte, K. K. Park, A. Nikoozadeh, and B. T. Khuri-Yakub, "Bandwidth and sensitivity optimization in CMUTs for airborne applications," in *Proc. IEEE Int. Ultrason. Symp.*, Chicago, IL, USA, Sep. 2014, pp. 166–169.

[5] N. Apte, K. K. Park, and B. T. Khuri-yakub, "Experimental evaluation of CMUTs with vented cavities under varying pressure," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Prague, Czech Republic, Jul. 2013, pp. 1724–1727.

[6] S. Anzinger, A. Fusco, D. Tumpold, C. Bretthauer, and A. Dehe, "Modeling of dual-backplate based airborne CMUTs with enhanced bandwidth," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Sep. 2020, pp. 1–4.

[7] B. Ma, K. Firouzi, K. Brenner, and B. T. Khuri-Yakub, "Wide bandwidth and low driving voltage vented CMUTs for airborne applications," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 66, no. 11, pp. 1777–1785, Nov. 2019.

[8] A. Frommhold, R. E. Palmer, and A. P. G. Robinson, "Spin-on carbon based on fullerene derivatives as hardmask materials for high-aspect-ratio etching," *J. Micro/Nanolithogr., MEMS, MOEMS*, vol. 12, no. 3, Jul. 2013, Art. no. 033003.

[9] T. Abe and Y. Itasaka, "Dry etching method using double-layered etching mask for modulating shape of deep-etched quartz surface," in *Proc. 16th Int. Solid-State Sens., Actuators Microsyst. Conf.*, Beijing, China, Jun. 2011, pp. 1508–1511.

[10] Z. Han, E. Salmi, M. Vehkamäki, M. Leskelä, and M. Ritala, "Metal oxide multilayer hard mask system for 3D nanofabrication," *Nanotechnology*, vol. 29, no. 5, Feb. 2018, Art. no. 055301.

[11] L. Li *et al.*, "Nanofabrication on unconventional substrates using transferred hard masks," *Sci. Rep.*, vol. 5, no. 1, pp. 1–6, Jul. 2015.

[12] H. A. C. Tilmans, "Equivalent circuit representation of electromechanical transducers: I. Lumped-parameter systems," *J. Micromech. Microeng.*, vol. 6, no. 1, pp. 157–176, 1996.

[13] I. Ladabaum, X. Jin, H. T. Soh, A. Atalar, and B. T. Khuri-Yakub, "Surface micromachined capacitive ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 45, no. 3, pp. 678–690, May 1998.

[14] W. P. Mason, *Electromechanical Transducers and Wave Filters*. Princeton, NJ, USA: Van Nostand, 1942.

[15] A. Lohfink and P.-C. Eccardt, "Linear and nonlinear equivalent circuit modeling of CMUTs," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 52, no. 12, pp. 2163–2172, Dec. 2005.

[16] A. Nikoozadeh, "Intracardiac ultrasound imaging using capacitive micromachined ultrasonic transducer (CMUT) arrays," Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, USA, 2010.

[17] B. Ma, C. Chang, H. K. Oğuz, K. Firouzi, B. T. Khuri-Yakub, and E. L. G. Lab, "Multi-parameter optimization of vented CMUTs for airborne applications," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Washington, DC, USA, Sep. 2017, pp. 1–4.

[18] D. Homentcovschi and R. N. Miles, "Modeling of viscous damping of perforated planar microstructures. Applications in acoustics," *J. Acoust. Soc. Amer.*, vol. 116, no. 5, pp. 2939–2947, Jul. 2004.

[19] D. Homentcovschi and R. N. Miles, "Viscous damping of perforated planar micromechanical structures," *Sens. Actuators A, Phys.*, vol. 119, no. 2, pp. 544–552, 2005.

[20] S. S. Mohite, H. Kesari, V. R. Sonti, and R. Pratap, "Analytical solutions for the stiffness and damping coefficients of squeeze films in MEMS devices with perforated back plates," *J. Micromech. Microeng.*, vol. 15, no. 11, pp. 2083–2092, Nov. 2005.

[21] W. S. Griffin, H. H. Richardson, and S. Yamanami, "A study of fluid squeeze-film damping," *J. Basic Eng.*, vol. 88, no. 2, pp. 451–456, Jun. 1966.

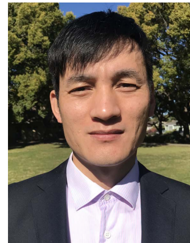
[22] K. K. Park, H. Lee, M. Kupnik, and B. T. Khuri-Yakub, "Fabrication of capacitive micromachined ultrasonic transducers via local oxidation and direct wafer bonding," *J. Microelectromech. Syst.*, vol. 20, no. 1, pp. 95–103, Feb. 2011.

[23] A. S. Erguri, Y. Huang, X. Zhuang, Ö. Oralkan, G. G. Yarahoglu, and B. T. Khuri-Yakub, "Capacitive micromachined ultrasonic transducers: Fabrication technology," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 52, no. 12, pp. 2242–2258, Dec. 2005.

[24] S. J. Cunningham and M. Kupnik, "Wafer bonding," in *MEMS Materials and Processes Handbook*. Boston, MA, USA: Springer, 2011, ch. 11, pp. 817–877.

[25] M. Kupnik, M.-C. Ho, S. Vaithilingam, and B. T. Khuri-Yakub, "CMUTs for air coupled ultrasound with improved bandwidth," in *Proc. IEEE Ultrason. Symp.*, Orlando, FL, USA, Oct. 2011, pp. 592–595.

[26] C. Bayram, S. Olcum, M. N. Senlik, and A. Atalar, "Bandwidth improvement in a cMUT array with mixed sized elements," in *Proc. IEEE Int. Ultrason. Symp.*, Rotterdam, The Netherlands, Sep. 2005, pp. 1956–1959.



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